Sustainable Wireless Network-on-Chip Architectures

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Sustainable Wireless Network-on-Chip Architectures focuses on developing novel Dynamic Thermal Management (DTM) and Dynamic Voltage and Frequency Scaling (DVFS) algorithms that exploit the advantages inherent in WiNoC architectures. The methodologies proposed—combined with extensive experimental validation—collectively represent efforts to create a sustainable NoC architecture for future many-core chips. Current research trends show a necessary paradigm shift towards green and sustainable computing. As implementing massively parallel energy-efficient CPUs and reducing resource consumption become standard, and their speed and power continuously increase, energy issues become a significant concern.

The need for promoting research in sustainable computing is imperative. As hundreds of cores are integrated in a single chip, designing effective packages for dissipating maximum heat is infeasible. Moreover, technology scaling is pushing the limits of affordable cooling, thereby requiring suitable design techniques to reduce peak temperatures. Addressing thermal concerns at different design stages is critical to the success of future generation systems. DTM and DVFS appear as solutions to avoid high spatial and temporal temperature variations among NoC components, and thereby mitigate local network hotspots.

- Defines new complex, sustainable network-on-chip architectures to reduce network latency and energy
- Develops topology-agnostic dynamic thermal management and dynamic voltage and frequency scaling techniques
- Describes joint strategies for network- and core-level sustainability
- Discusses novel algorithms that exploit the advantages inherent in Wireless Network-on-Chip architectures

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